Realizing the Potential of Silicon Carbide for Power Electronics

Sponsored by Fiven

Panelists

Moderator:

Rosario Gerhardt
Professor
Georgia Institute of Technology

Panelists:

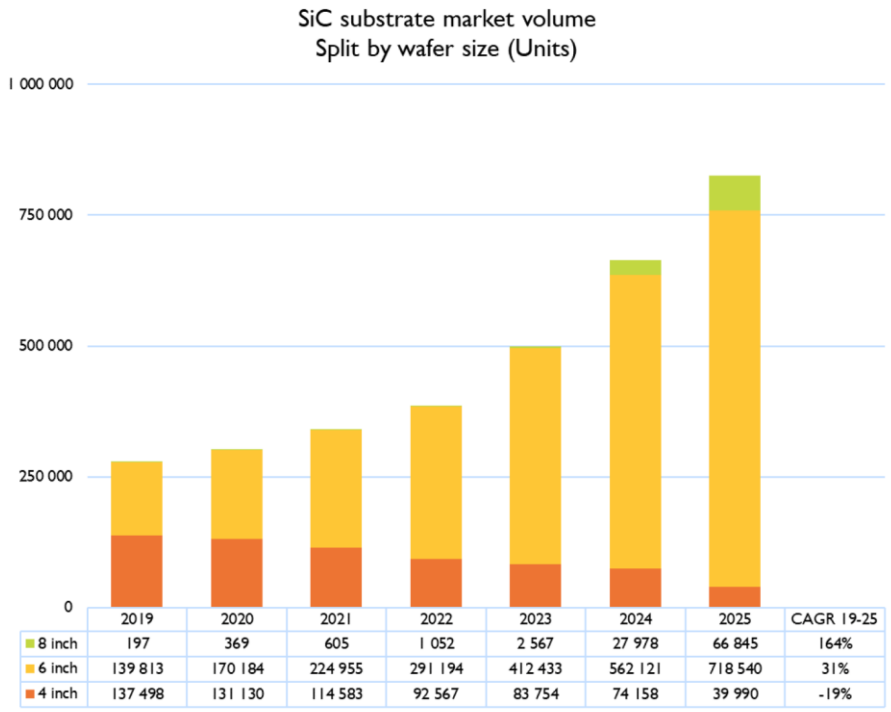
Wei Fan
Director of Global Ceramics Technology
Momentive Technologies

Robert Rhoades
President & CTO
X-trinSiC

SiC Market – Semiconductor Applications

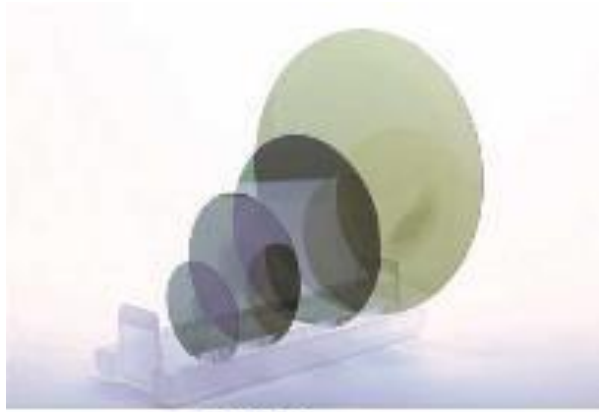
- **Explosive growth in EV, 5G and power devices for energy efficient systems**

- Power Devices (MOSFETs & diodes)
- EV - Power inverters for drive train and supercharging stations
  - Provides >20% increase in range from same batteries
  - Enables higher voltage & power for 3x faster charging
- 5G communications

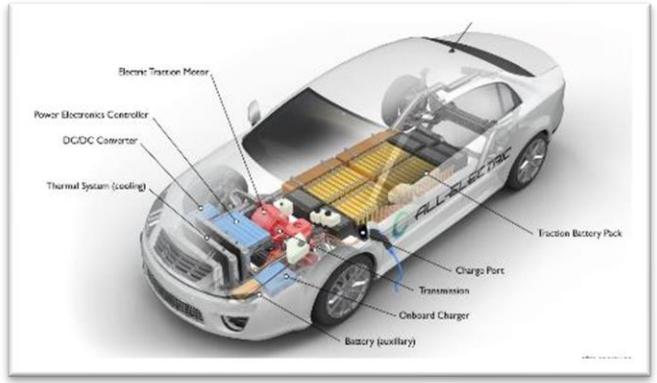


	2019	2020	2021	2022	2023	2024	2025	CAGR 19-25
8 inch	197	369	605	1 052	2 567	27 978	66 845	164%
6 inch	139 813	170 184	224 955	291 194	412 433	562 121	718 540	31%
4 inch	137 498	131 130	114 583	92 567	83 754	74 158	39 990	-19%

SiC Substrate Demand by Year
(Yole Report 2021)



4H N-type



SiC requires advanced equipment and process expertise

- Extremely hard and chemically inert
- Long process times for nearly every process (saw, grind, polish)
- Previous experience with Si or III-V materials does not transfer easily
- Material properties force adaptation of equipment & process methods

Why Use SiC?

Compared to traditional silicon

>50% Improved **Efficiency**

15x Higher **Breakdown Voltage**

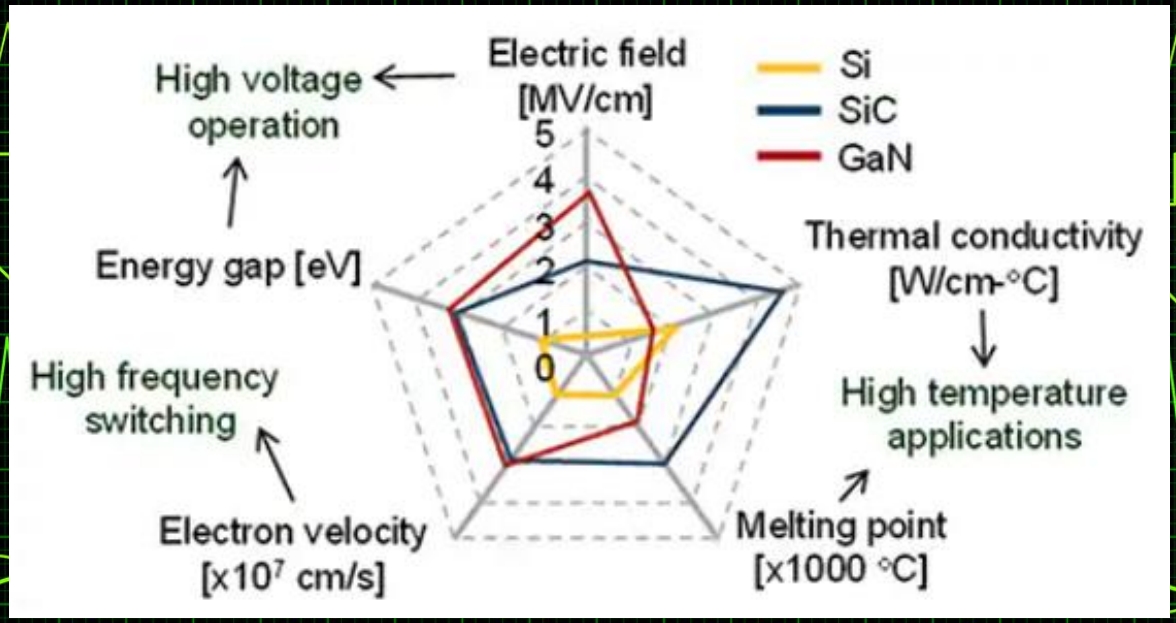
>65% Higher **Power Density**

2-3x Faster **Switching Speeds**

Modules are **Smaller and Lighter**

3x Better **Heat Dissipation**

Higher **Temperature Tolerance**
(less cooling required)

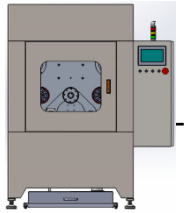


Source: Digikey (web site)

Source: ROHM EV racing team (web site)

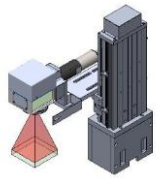
Process Sequence for SiC Wafering

Input
SiC Puck

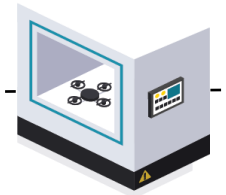


Slice
Wiresaw

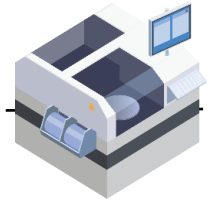
Clean
Megasonic



Mark
Laser

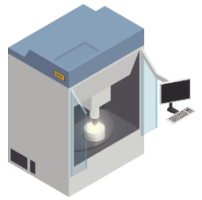


Edge
Edge Grind



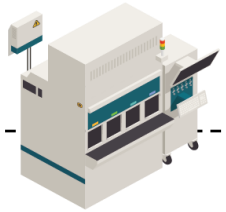
Planarize
If needed

Clean
Various

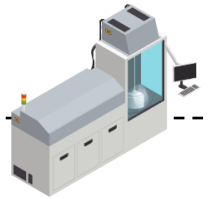


Grind
Both sides

Clean
Megasonic

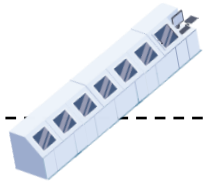


CMP
Both sides



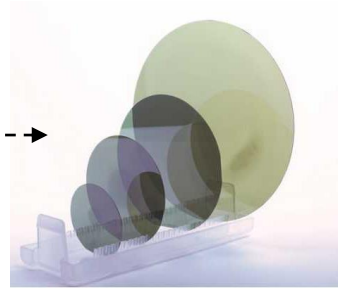
Clean
DS Scrub

Measure
Shape



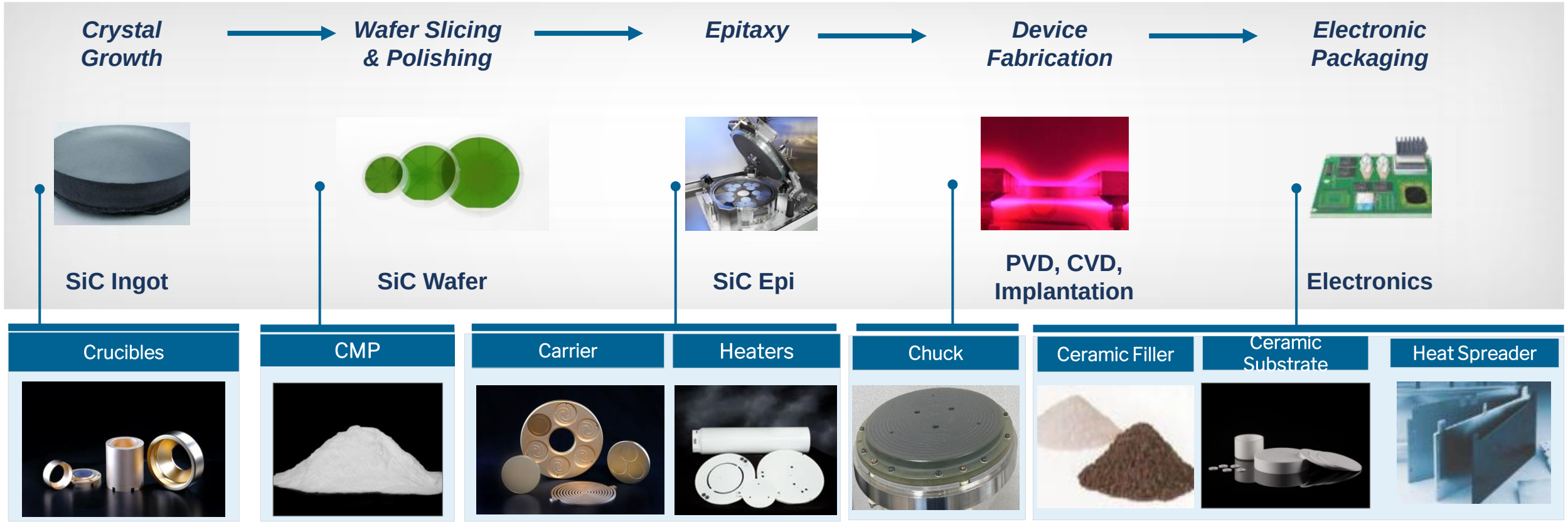
Final Cln
Clean Line

Measure
Defectivity



Output
SiC Wafers

Ceramics in Wide-Bandgap Semiconductor Processing



MOMENTIVE® TECHNOLOGIES

SiC Wafers - Target Specifications

PARAMETER	UNITS	100mm Wafers	150mm Wafers	200mm Wafers
Thickness	μm	325-550	325-550	450-550
THK Variation	μm	± 5	± 5	± 5
TTV	μm	<3	<5	<5
Bow Degradation*	μm	<10	<15	<20
Warp Degradation*	μm	<10	<15	<20
Surface Ra**	nm	<0.3 (Si-face)	<0.3 (Si-face)	<0.3 (Si-face)
Defects (LPD's)	#	<100	<150	<200
5x5 LTV Yield***	%	90%	90%	85%

* Wafer shape depends on more than grind and polish. It is a strong function of internal stresses and factors related to crystal growth.

** As measured by white light interferometer over a 250x350um area. This is also somewhat dependent on material quality. Polytype inclusions, low angle grain boundaries, and micropipes may increase the Ra measurement.

***Note: Material quality will impact this. Polytype inclusions, micropipes, or doping bands will negatively impact this measurement.